

Appln No. 10/737,416
Amtd. dated October 27, 2005
Reply to Office Action of June 19, 2005

PATENT

Amendments to the Specification:

Please replace paragraph 26 with the following amended paragraph:

[0026] Concurrent references are made to Figs. 2 and 3 below. Resistor 28 of replication 200 replicates (i.e., mimics) half of load resistor R_L of Fig. 2. NMOS transistor 30 replicates either of NMOS transistor 8 and 10, whichever is in a conducting state. DC current source 26 replicates current I_0 flowing through NMOS transistor 2. In order to minimize the power consumption, the transistors and resistor in replication circuit 200 are selected so as to operate at a current level of I_0/M , where M is a positive number greater than unity. Thus, replica resistor 28 of Fig. 3 is selected to have a resistance of $M^*R_L/2$. Similarly, the ratio of the channel-width to channel-length $(W/L)_{30}$ of replica NMOS transistor 30 of Fig. 3 is selected so as to be equal to $(W/L)_s/M$, where $(W/L)_s$ is the ratio of the channel-width to channel-length of the replicated NMOS transistors 8 and 10. Since transistor 30 is adapted to replicate either transistor 8 or transistor 10 when it is in a conducting state, the gate terminal of transistor 30 is coupled to the positive voltage supply terminal. Replica PMOS transistor 32 replicates PMOS transistor 12 of Fig. 2. Accordingly, the ratio of the channel-width to channel-length $(W/L)_{32}$ of replica PMOS transistor 32 of Fig. 3 is selected so as to be equal to $(W/L)_{12}/M$, where $(W/L)_{12}$ is the ratio of the channel-width to channel-length of the replicated PMOS transistor 12.

Please replace paragraph 29 with the following amended paragraph:

[0029] Fig. 4 shows a schematic diagram of LVDS transmitter circuit 300 that is formed by coupling replication circuit 200 to LVDS output driver circuit 100. As seen from Fig. 4, LVDS transmitter 300 receives, in part, a second voltage supply $[[V_{dd}]]$ that supplies a voltage to, e.g., NMOS transistor 2, and voltage supply V_{ROS} that supplies a voltage to the non-inverting input terminals of OTAs 20 and 34. Output voltages generated and delivered to output terminals A and

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B comply with the TIA/EIA-644-A. The voltage applied to the non-inverting input terminal of OTA 22 is supplied by replication circuit 200.